FIG. 1

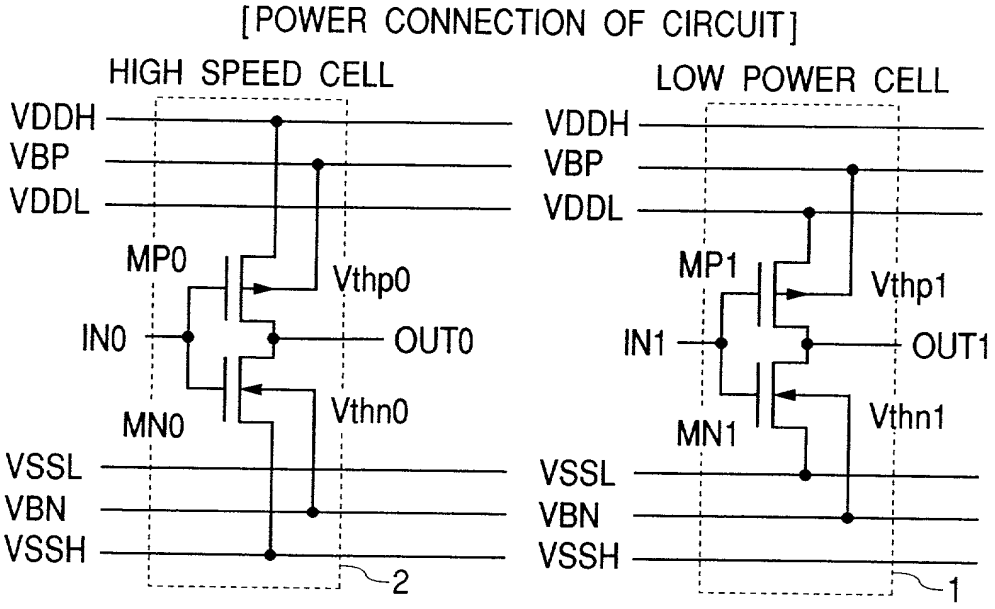


FIG. 2

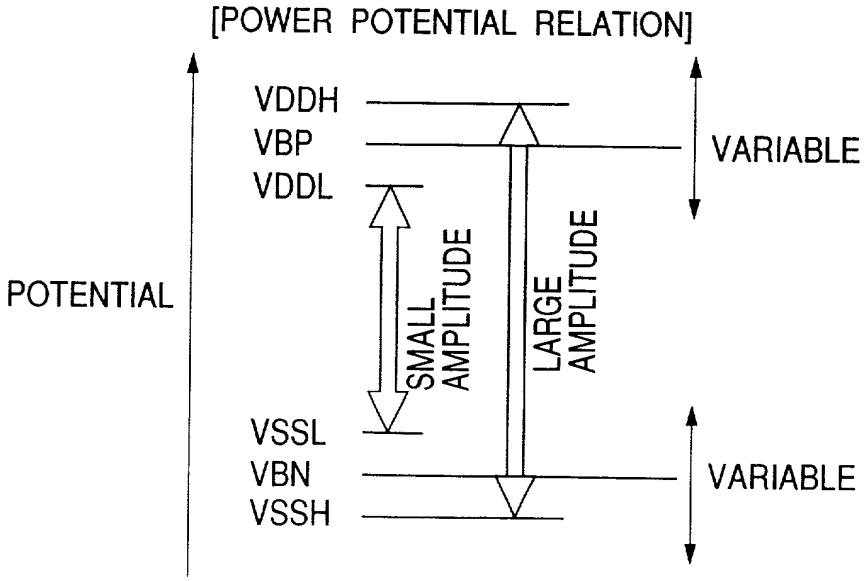


FIG. 3

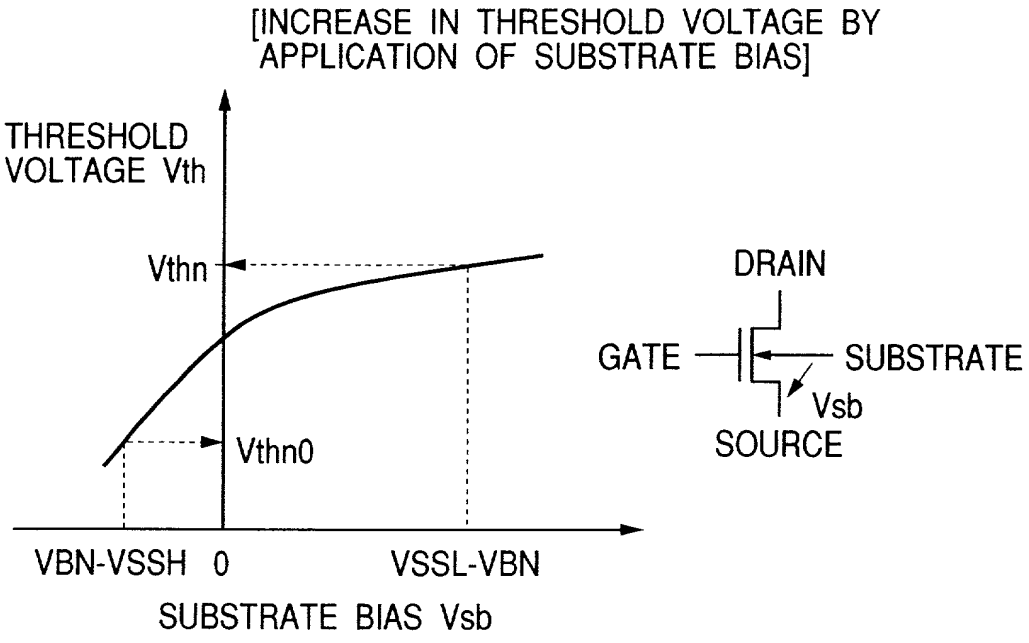

[INCREASE IN THRESHOLD VOLTAGE BY APPLICATION OF SUBSTRATE BIAS]
THRESHOLD VOLTAGE Vth
Vthn
Vthn0
VBN-VSSH
0
VSSL-VBN
SUBSTRATE BIAS Vsb
DRAIN
GATE
SUBSTRATE
Vsb
SOURCE

FIG. 4

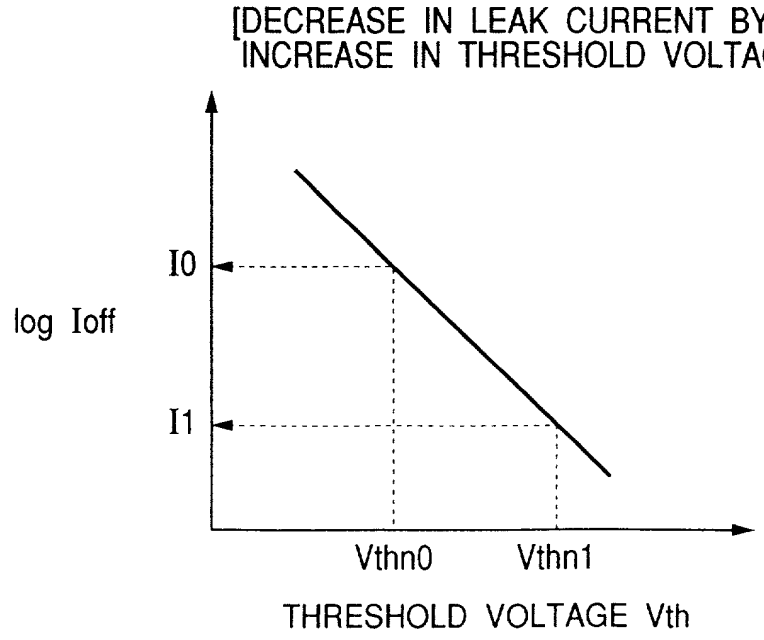

[DECREASE IN LEAK CURRENT BY INCREASE IN THRESHOLD VOLTAGE]
log Ioff
I0
I1
Vthn0
Vthn1
THRESHOLD VOLTAGE Vth

FIG. 5

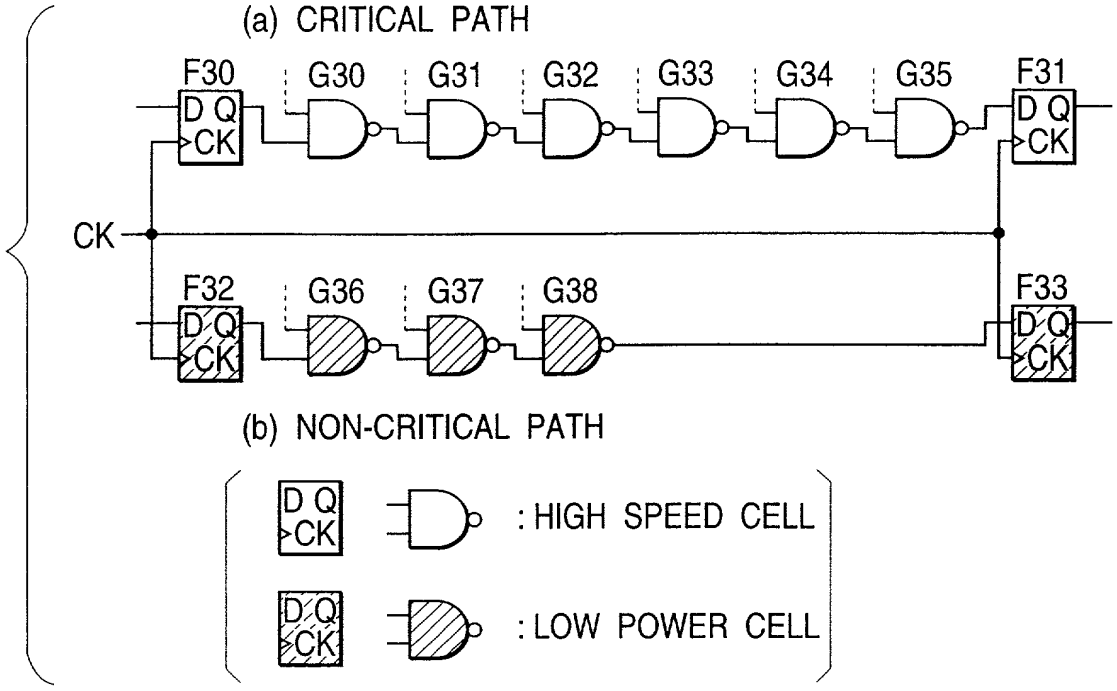


FIG. 6

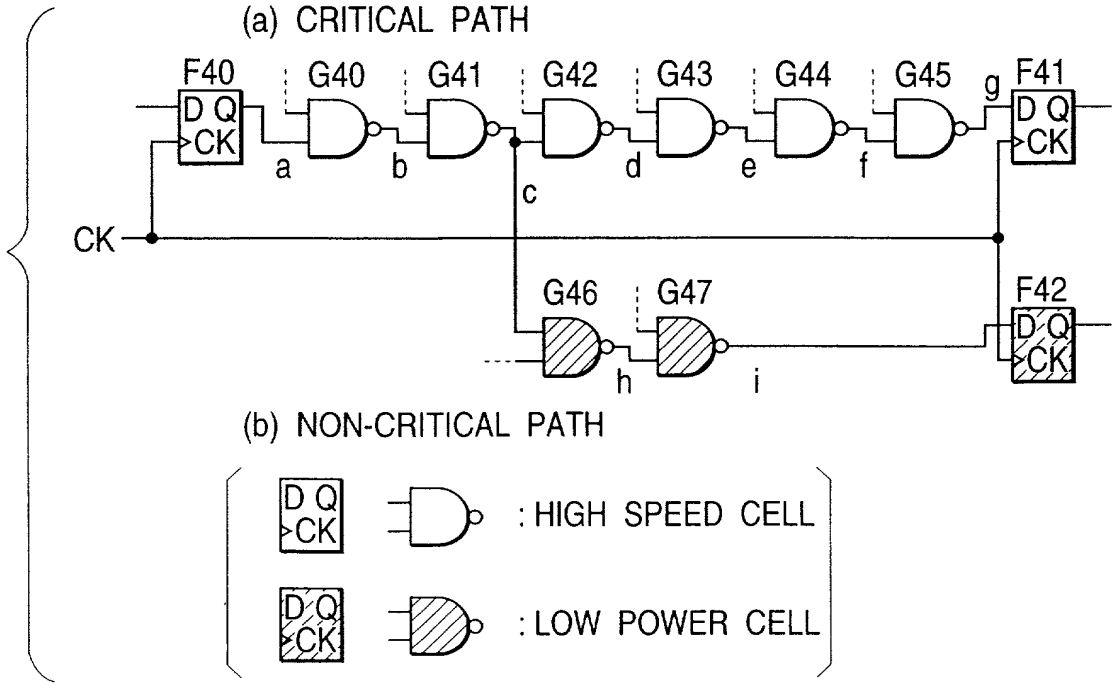
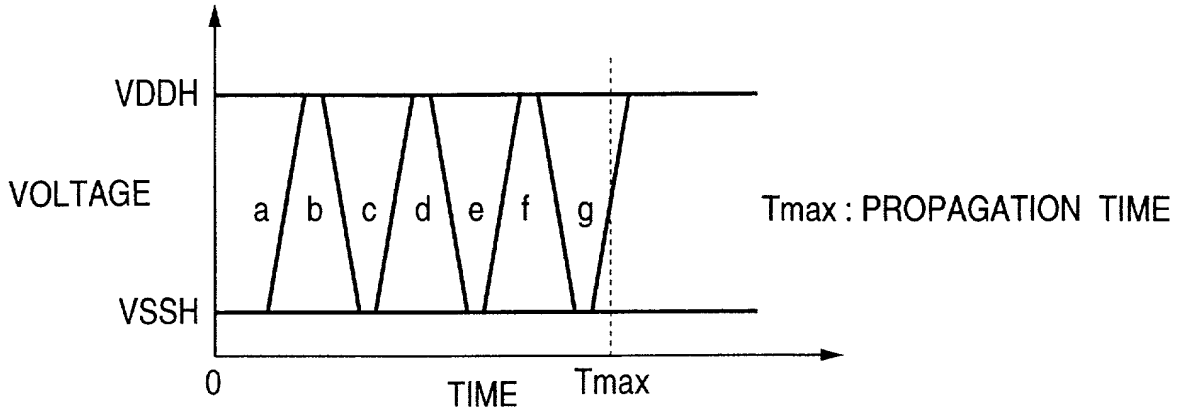
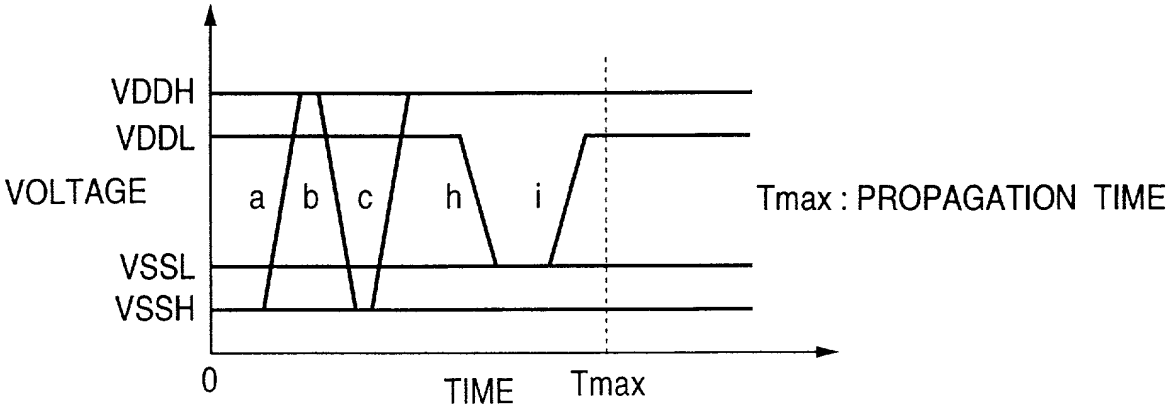


FIG. 7(A)



OPERATION WAVEFORM OF CRITICAL PATH

FIG. 7(B)



OPERATION WAVEFORM OF NON-CRITICAL PATH

FIG. 8

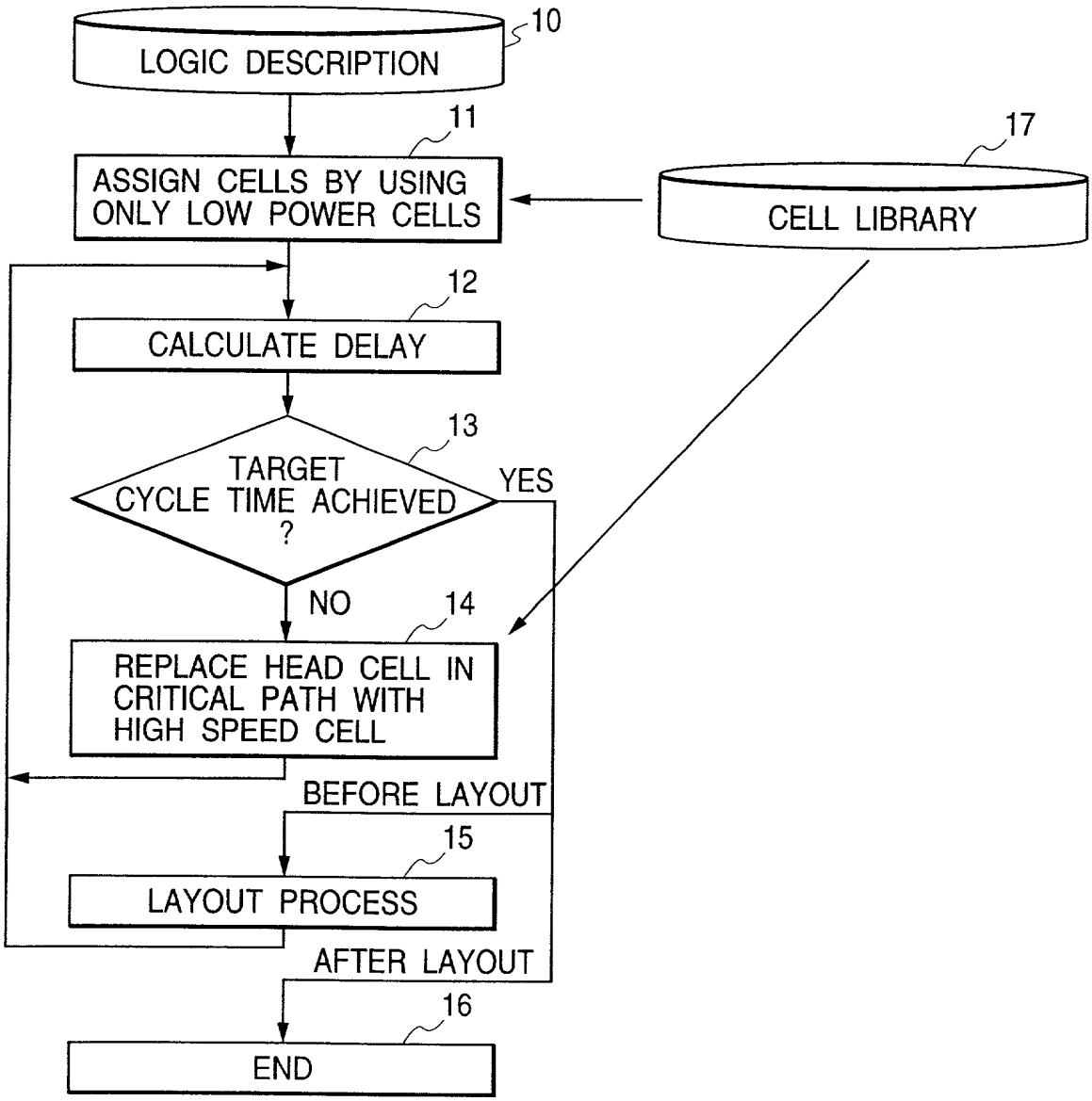

LOGIC DESCRIPTION
10
ASSIGN CELLS BY USING ONLY LOW POWER CELLS
11
CELL LIBRARY
17
CALCULATE DELAY
12
TARGET CYCLE TIME ACHIEVED ?
13
YES
NO
REPLACE HEAD CELL IN CRITICAL PATH WITH HIGH SPEED CELL
14
BEFORE LAYOUT
LAYOUT PROCESS
15
AFTER LAYOUT
END
16

FIG. 9(A)

[CASE USING ONLY LOW POWER CELLS]

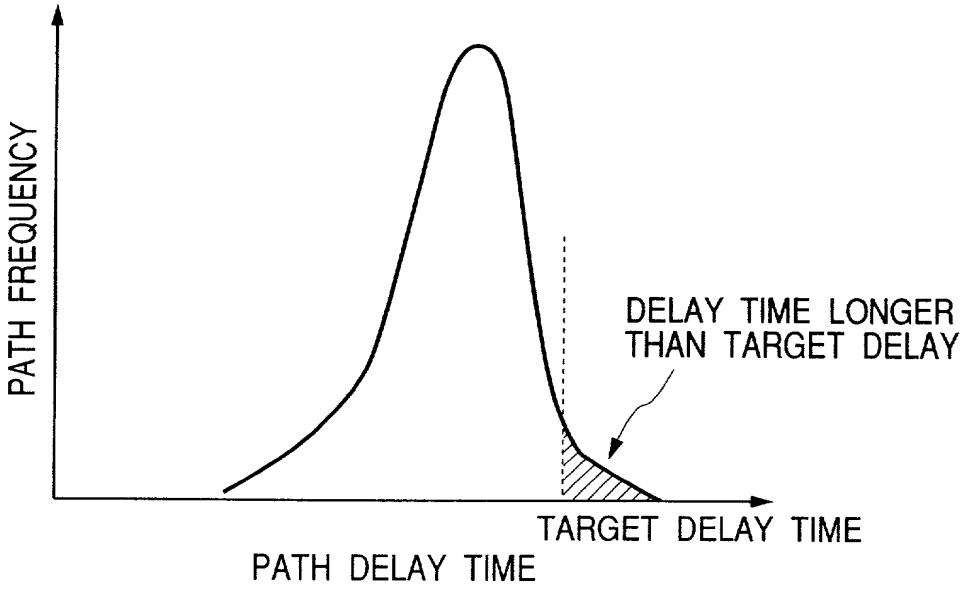


FIG. 9(B)

[CASE USING HIGH SPEED CELL FOR CRITICAL PATH]

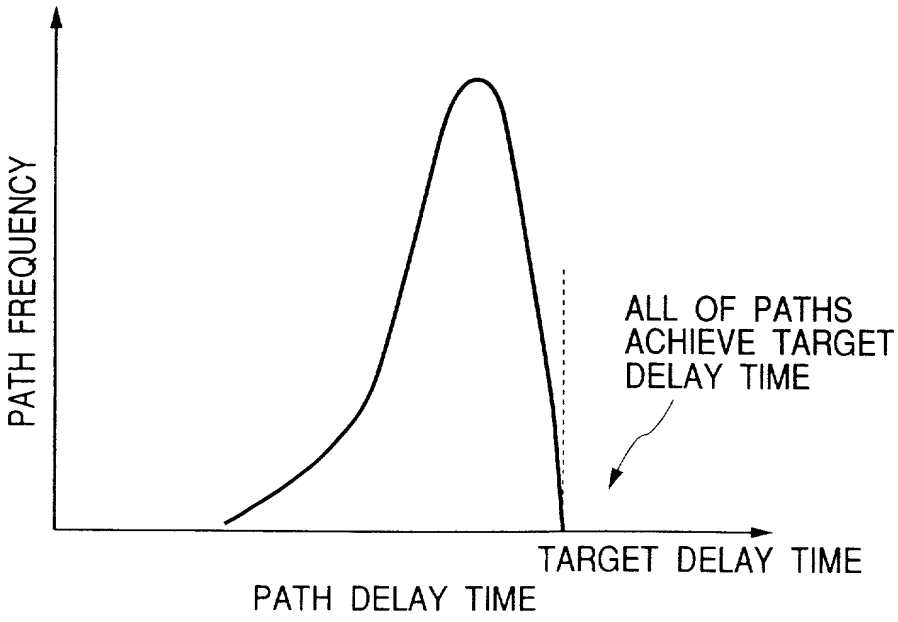


FIG. 10(A)

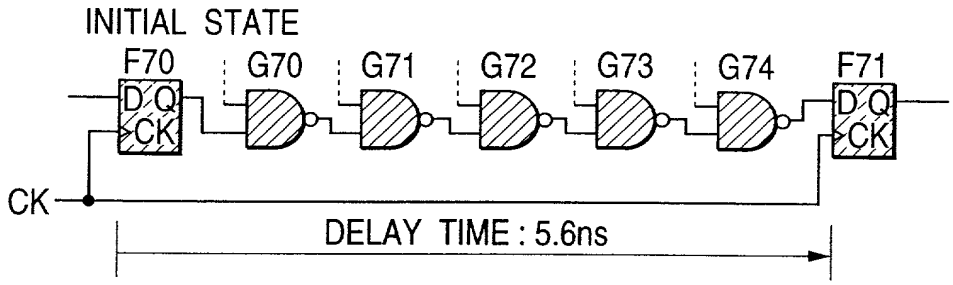


FIG. 10(B)

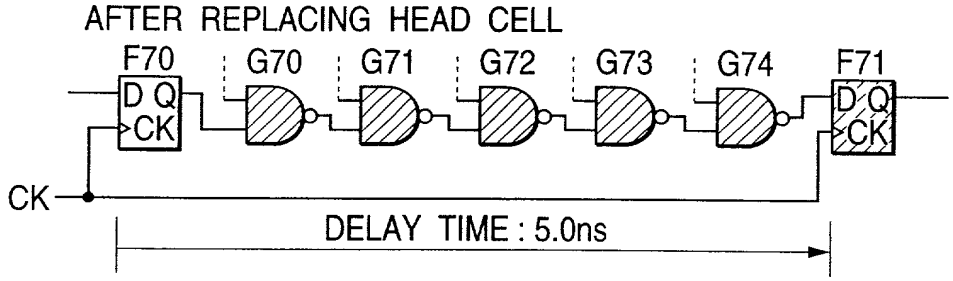


FIG. 10(C)

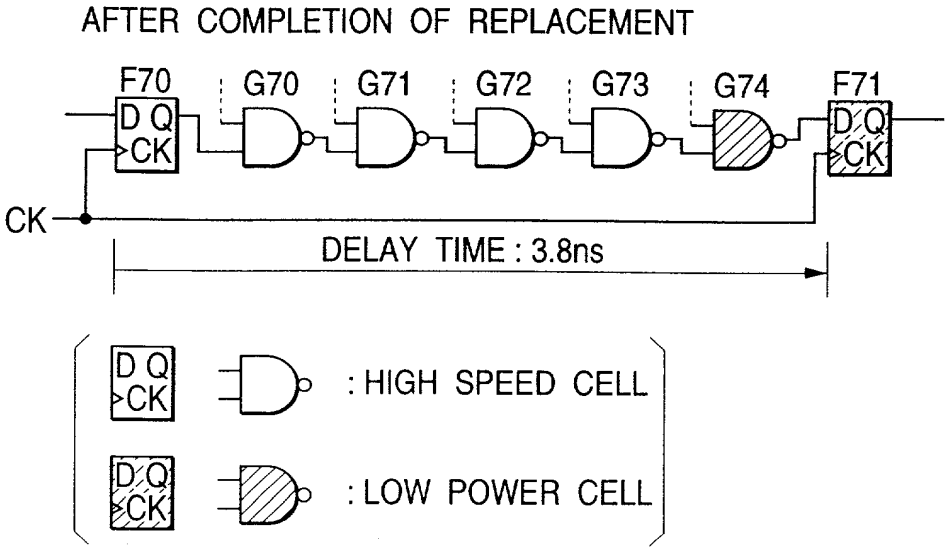


FIG. 11

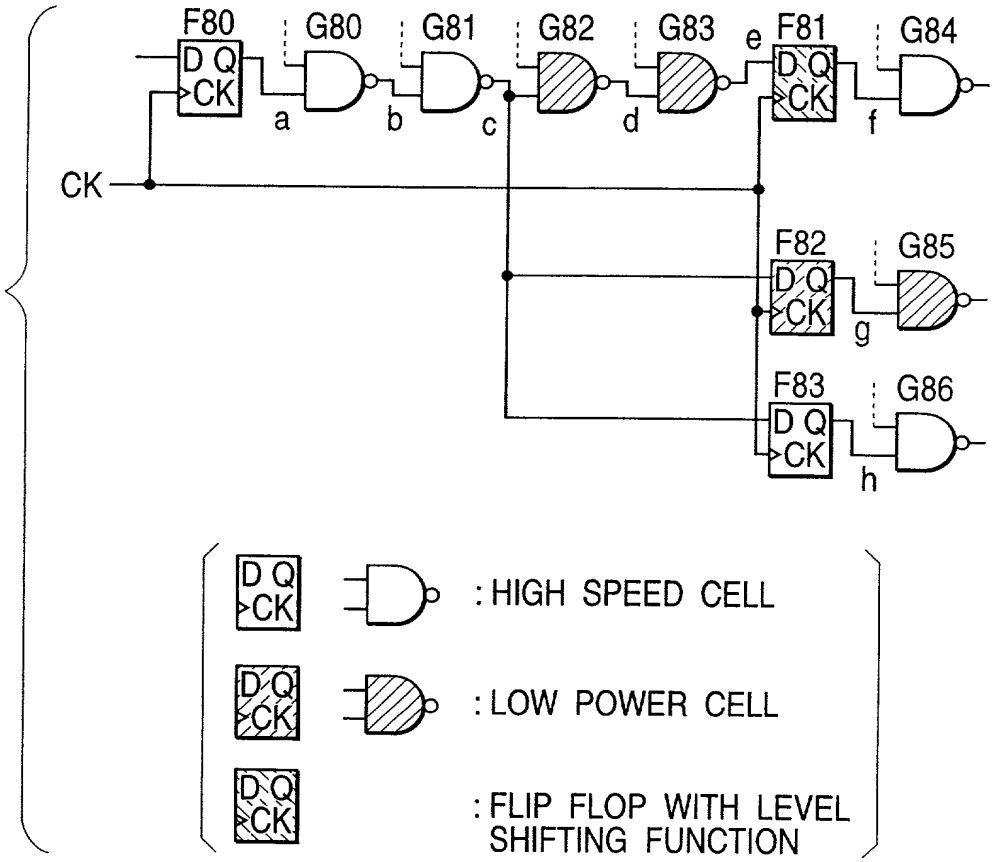

F80
G80
G81
G82
G83
e
F81
G84
D Q
CK
a
b
c
d
f
CK
F82
G85
g
F83
G86
h
: HIGH SPEED CELL
: LOW POWER CELL
: FLIP FLOP WITH LEVEL SHIFTING FUNCTION

FIG. 12

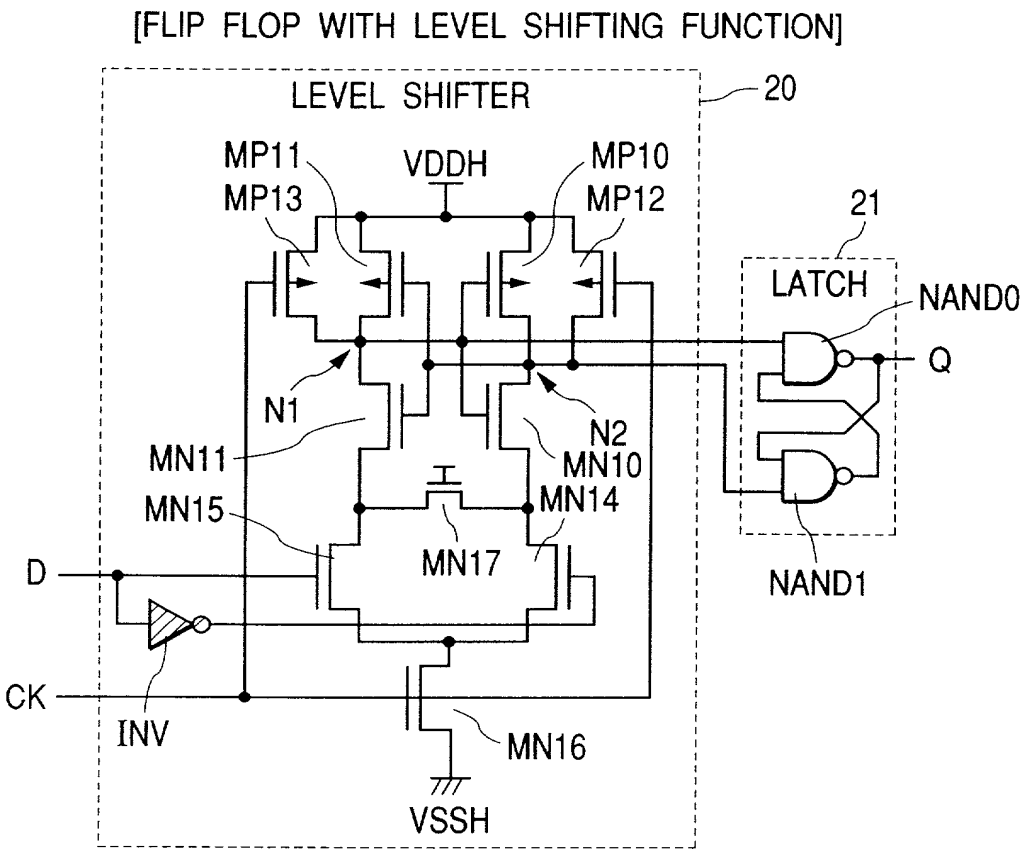

[FLIP FLOP WITH LEVEL SHIFTING FUNCTION]
LEVEL SHIFTER
20
MP11
MP13
VDDH
MP10
MP12
21
LATCH
NAND0
Q
N1
N2
MN11
MN10
MN15
MN14
MN17
D
NAND1
CK
INV
MN16
VSSH

FIG. 13

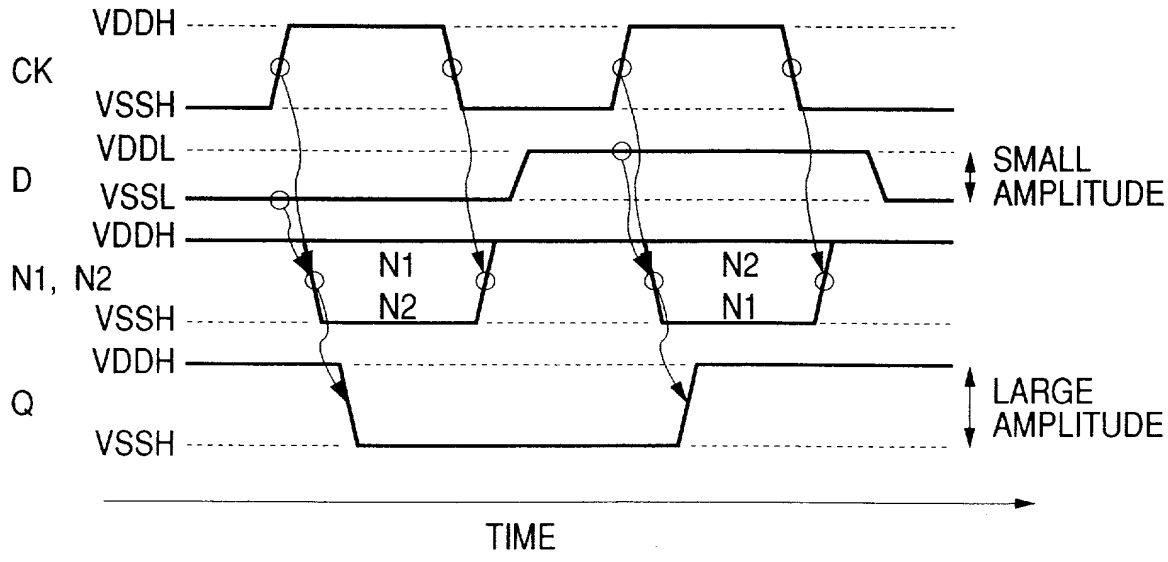

VDDH
CK
VSSH
VDDL
D
VSSL
SMALL AMPLITUDE
VDDH
N1, N2
N1
N2
N2
N1
VSSH
VDDH
Q
LARGE AMPLITUDE
VSSH
TIME

FIG. 14

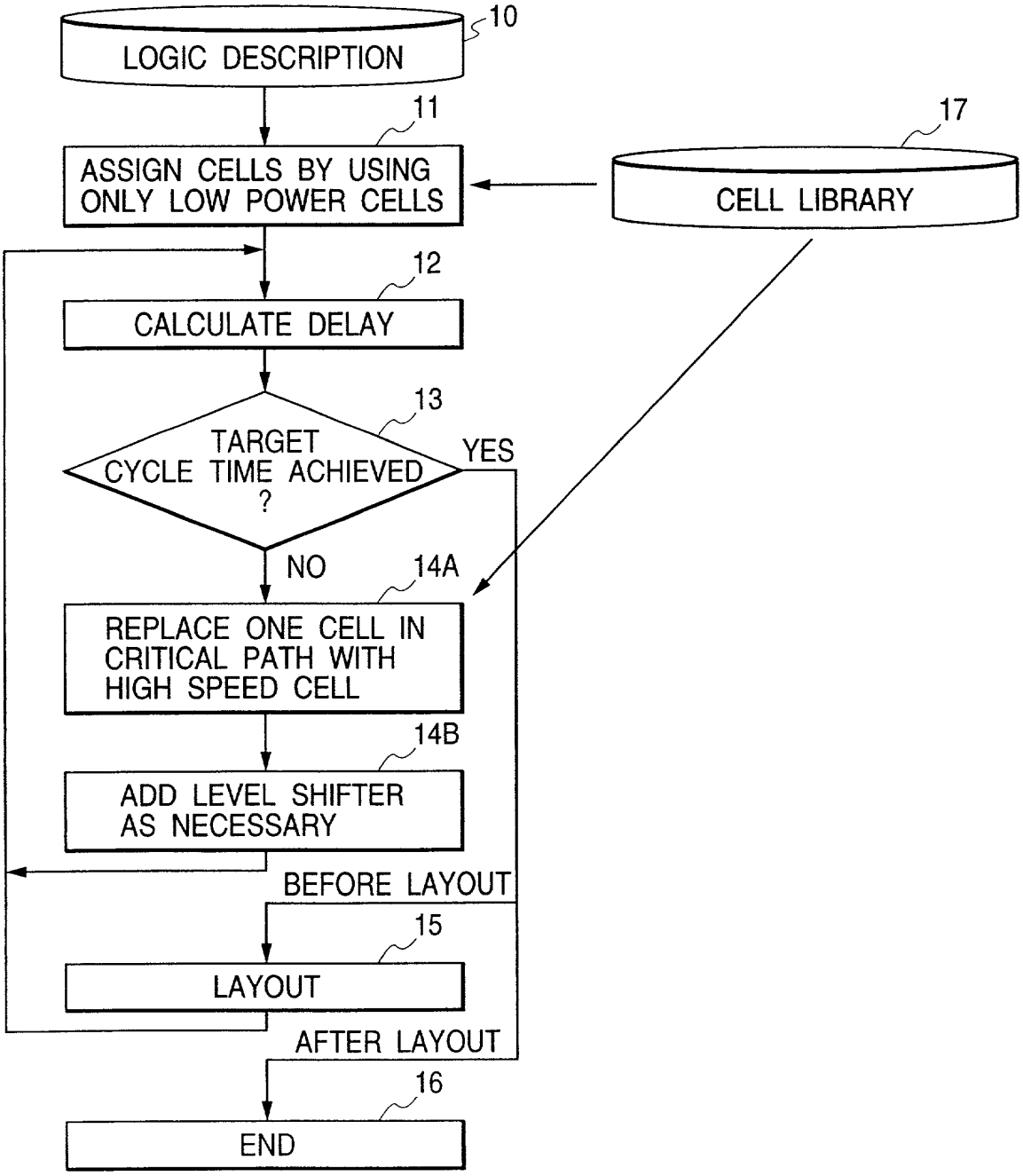

LOGIC DESCRIPTION
10
11
ASSIGN CELLS BY USING ONLY LOW POWER CELLS
17
CELL LIBRARY
12
CALCULATE DELAY
13
TARGET CYCLE TIME ACHIEVED ?
YES
NO
14A
REPLACE ONE CELL IN CRITICAL PATH WITH HIGH SPEED CELL
14B
ADD LEVEL SHIFTER AS NECESSARY
BEFORE LAYOUT
15
LAYOUT
AFTER LAYOUT
16
END

FIG. 15(A)

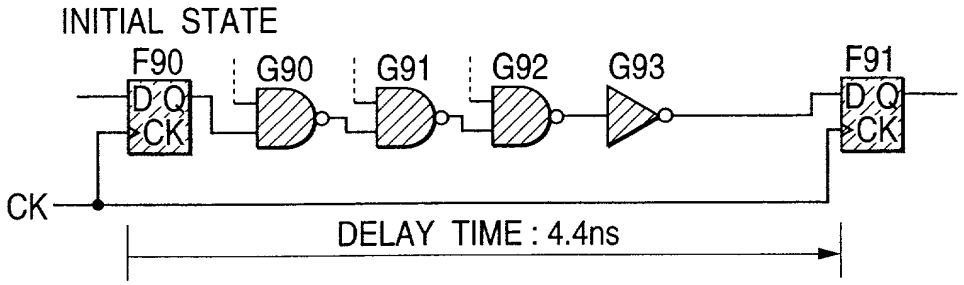


FIG. 15(B)

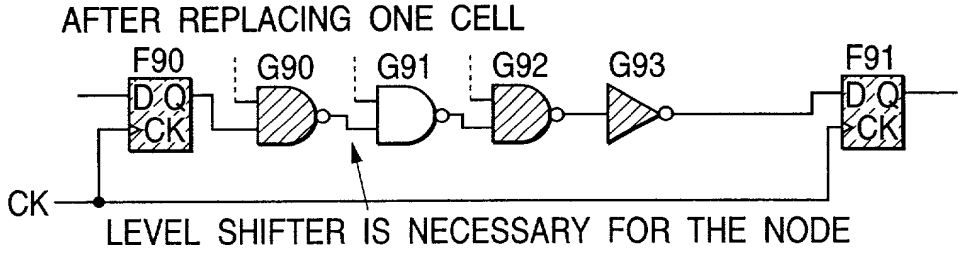


FIG. 15(C)

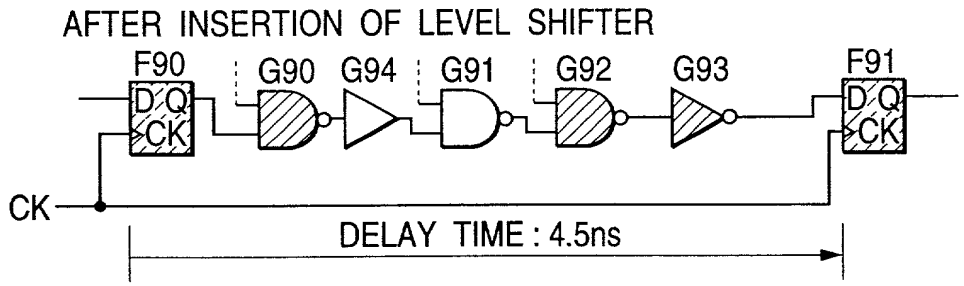


FIG. 15(D)

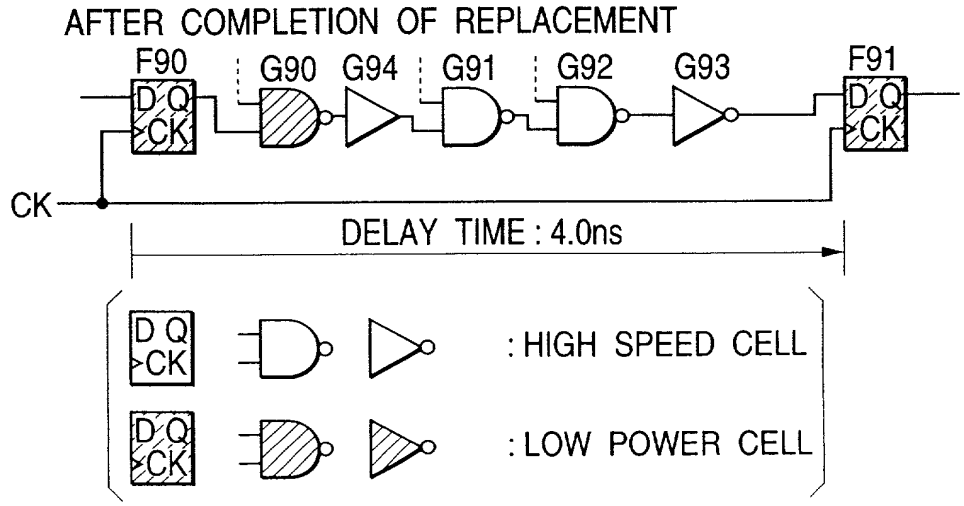


FIG. 16

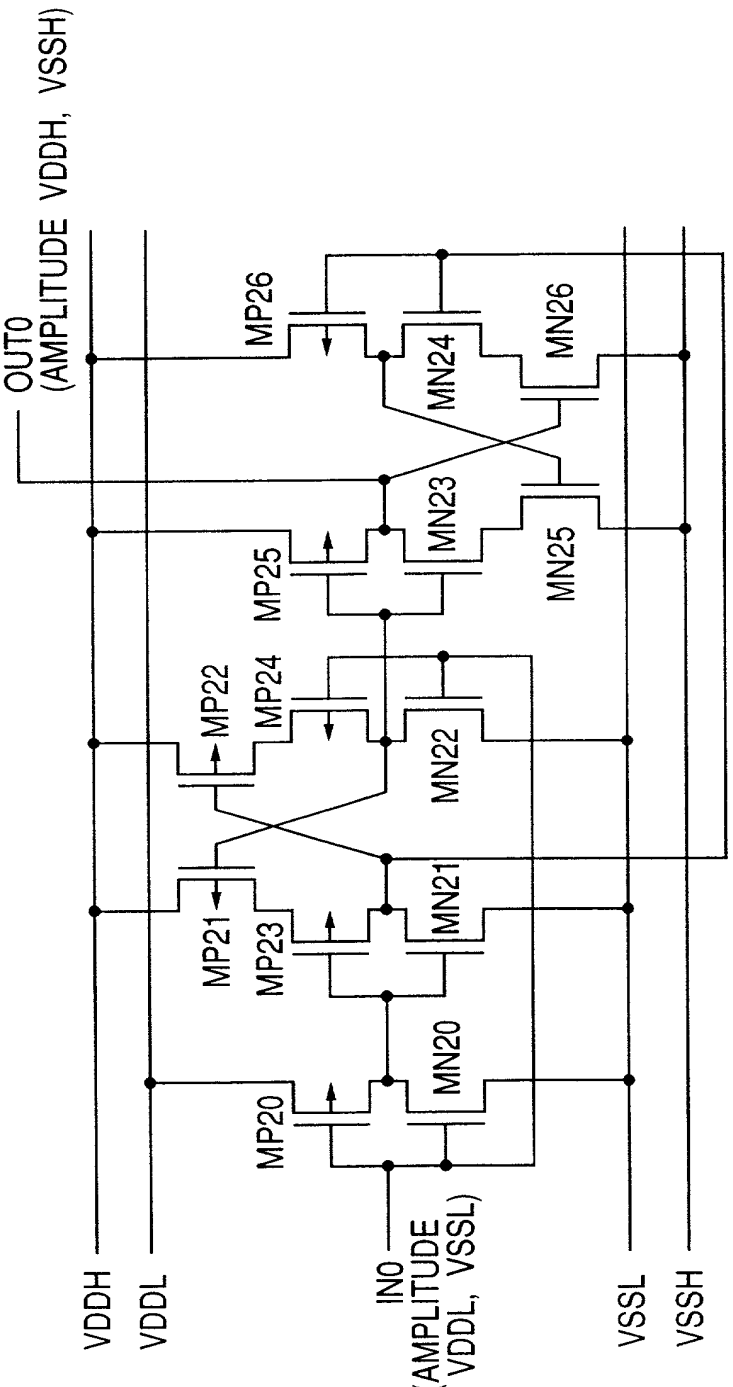

OUT0
(AMPLITUDE VDDH, VSSH)
MP26
MN24
MN26
MP25
MN23
MN25
MP22
MP24
MN22
MP21
MP23
MN21
MP20
MN20
VDDH
VDDL
IN0
(AMPLITUDE
VDDL, VSSL)
VSSL
VSSH

FIG. 17

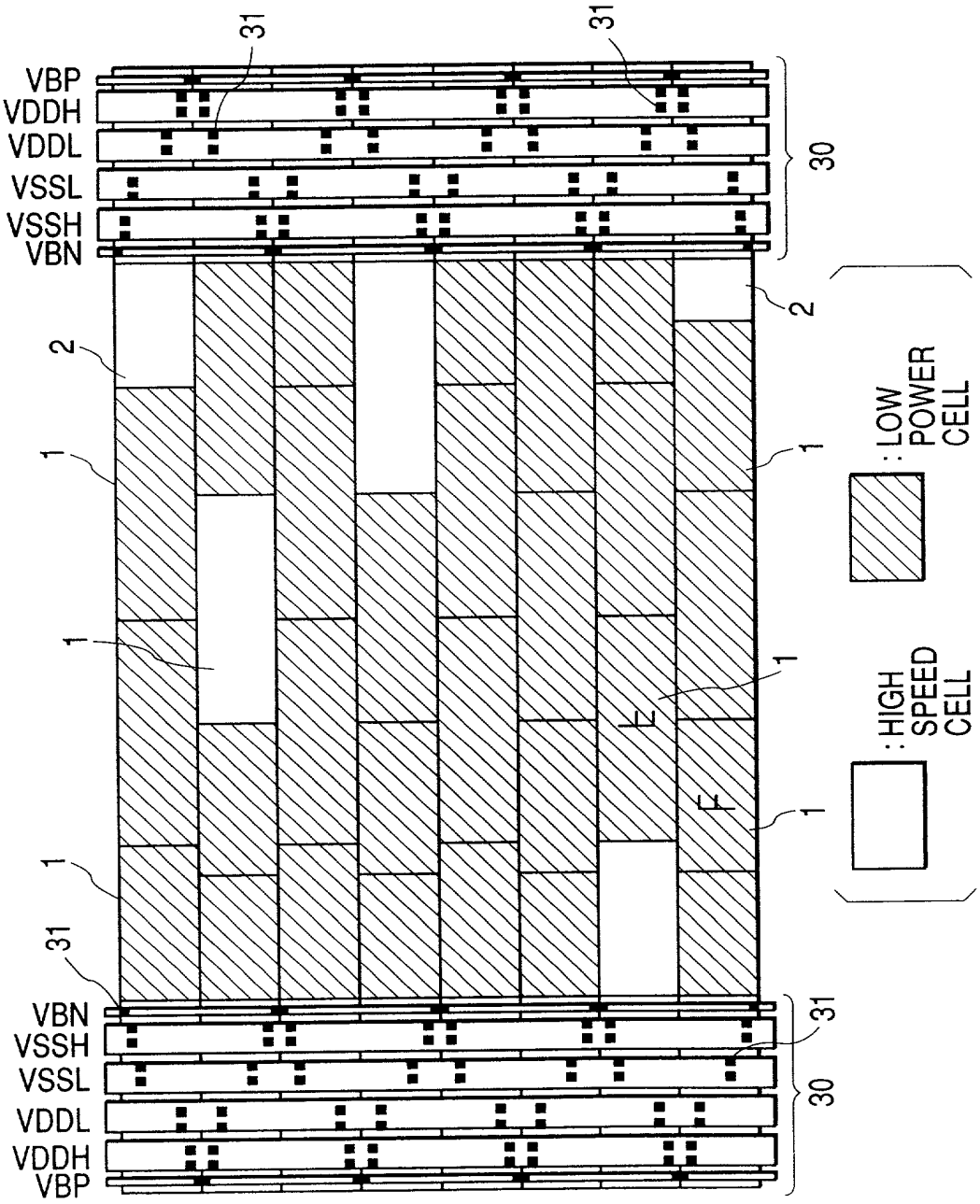

VBP
VDDH
VDDL
VSSL
VSSH
VBN
31
30
2
1
E
F
: LOW POWER CELL
: HIGH SPEED CELL

FIG. 18

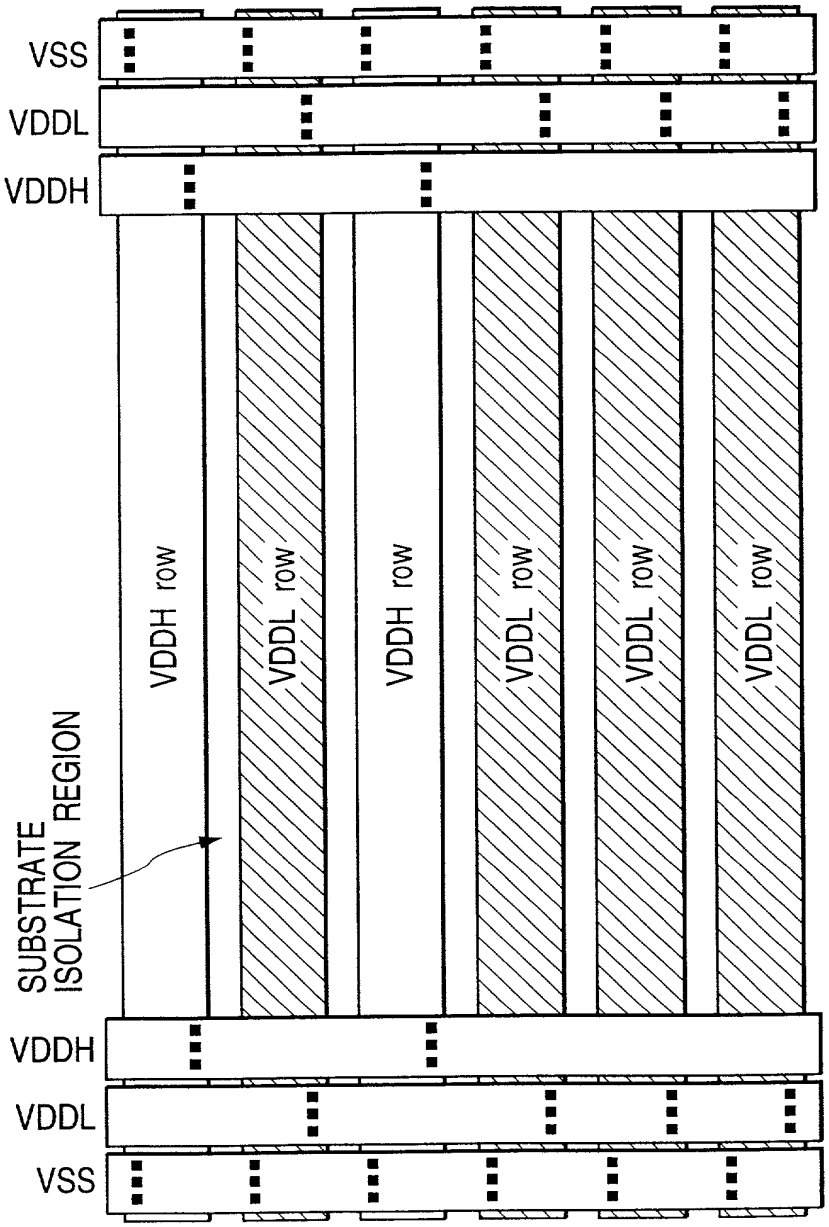

VSS
VDDL
VDDH
VDDH row
VDDL row
VDDH row
VDDL row
VDDL row
VDDL row
SUBSTRATE ISOLATION REGION
VDDH
VDDL
VSS

FIG. 19(A)

[CONVENTIONAL CELL LAYOUT]

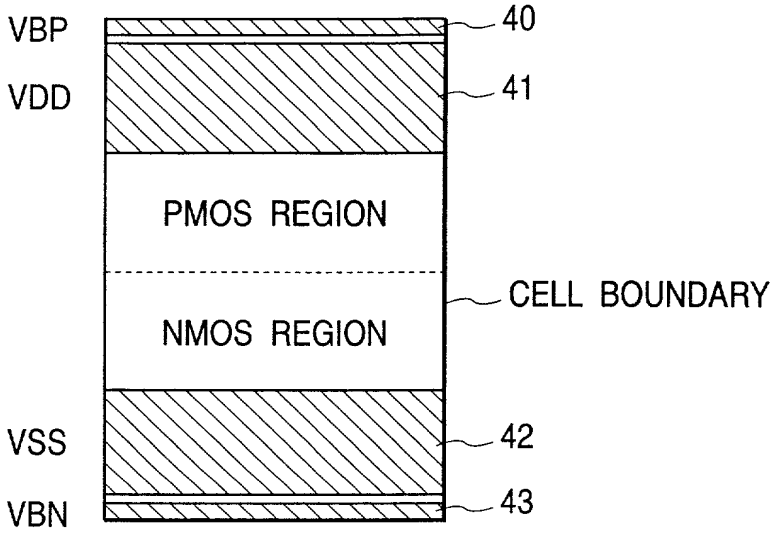


FIG. 19(B)

[CELL LAYOUT OF THE INVENTION]

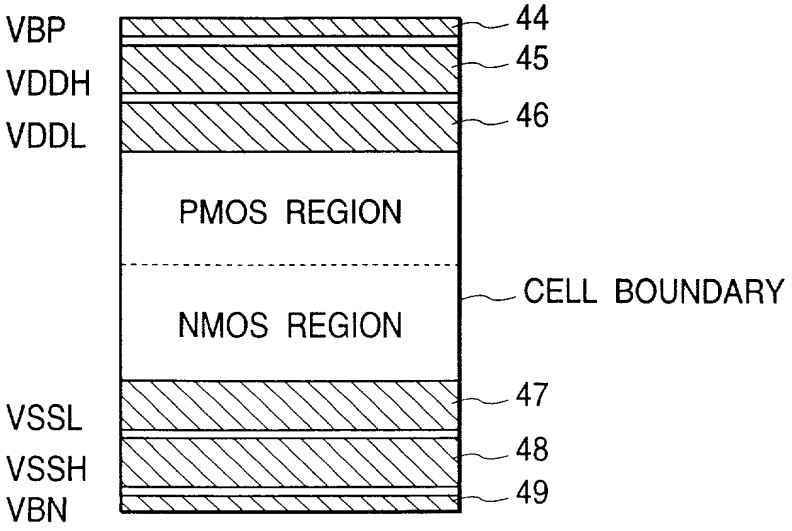


FIG. 20(A)

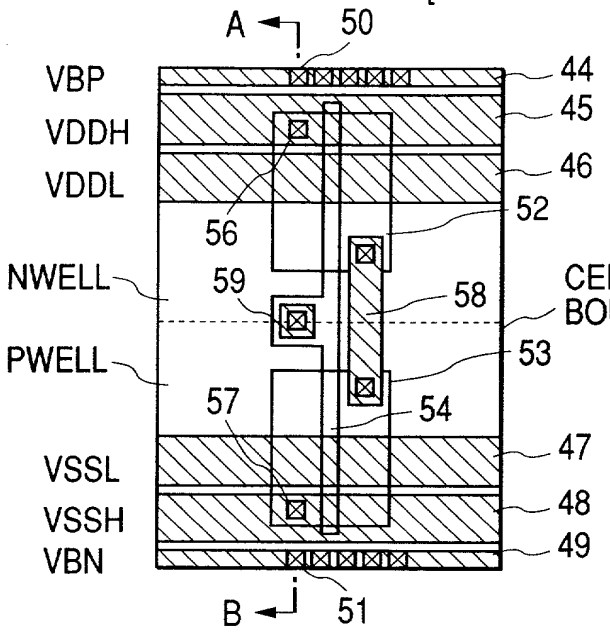


FIG. 20(B)

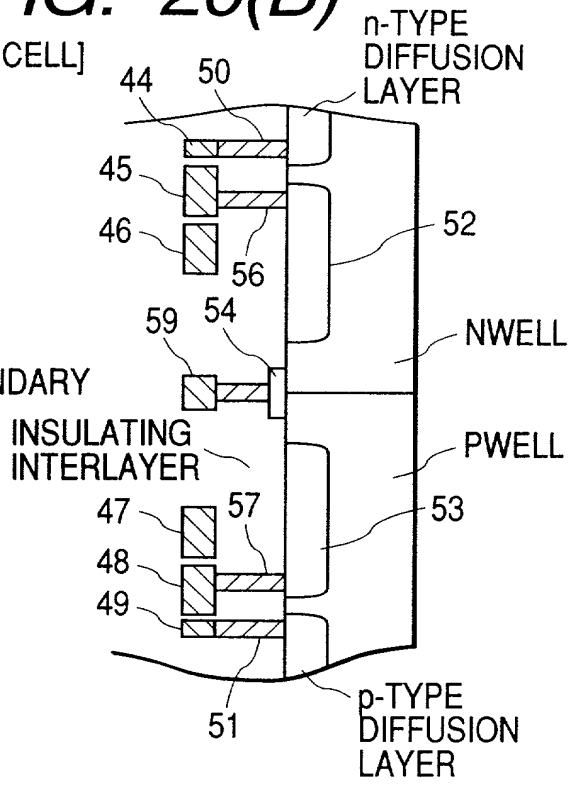


FIG. 21(A)

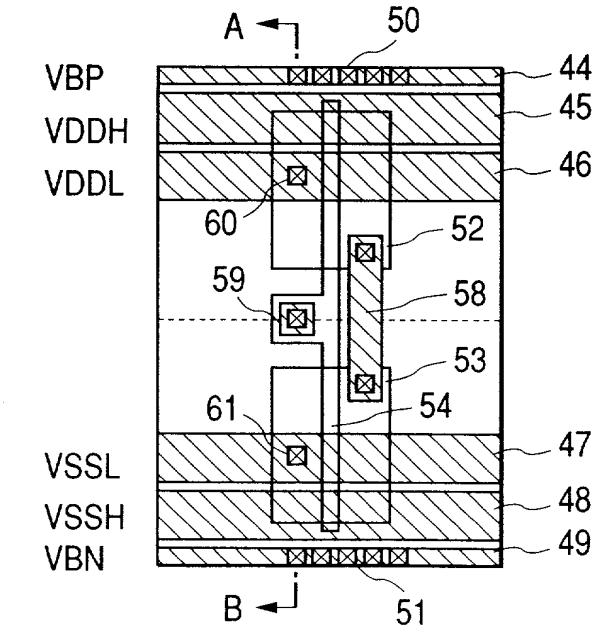


FIG. 21(B)

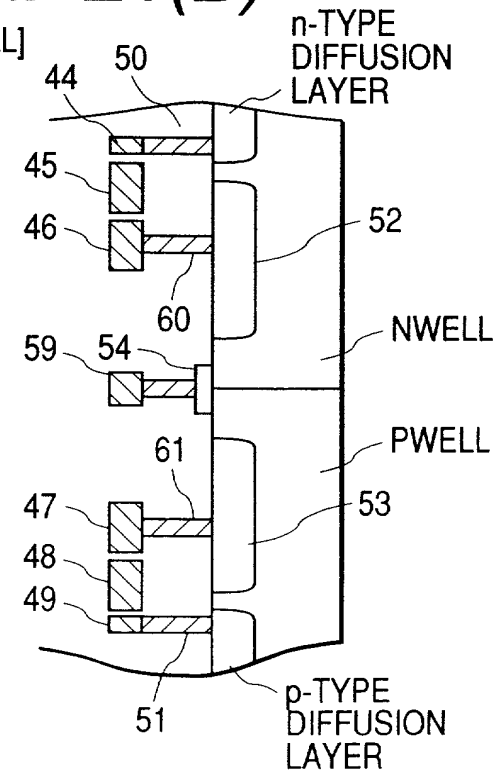


FIG. 22

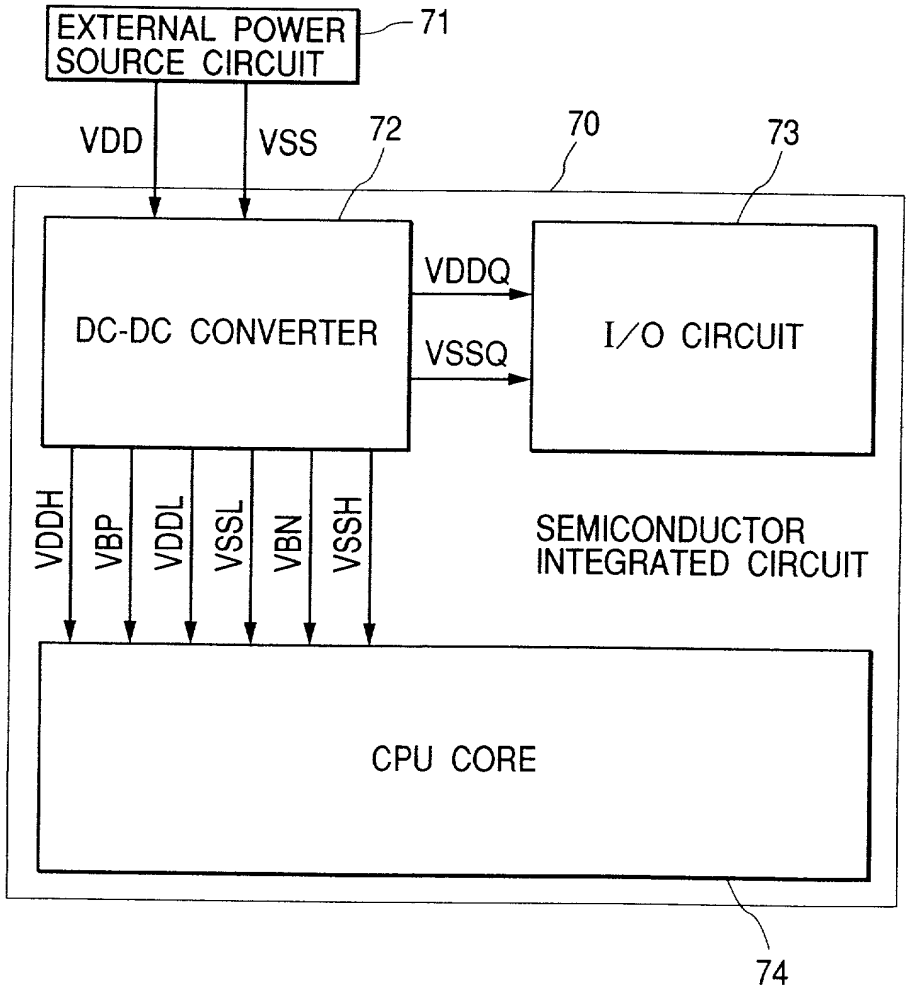

EXTERNAL POWER SOURCE CIRCUIT
71
VDD
VSS
72
70
73
DC-DC CONVERTER
VDDQ
VSSQ
I/O CIRCUIT
VDDH
VBP
VDDL
VSSL
VBN
VSSH
SEMICONDUCTOR INTEGRATED CIRCUIT
CPU CORE
74

FIG. 23

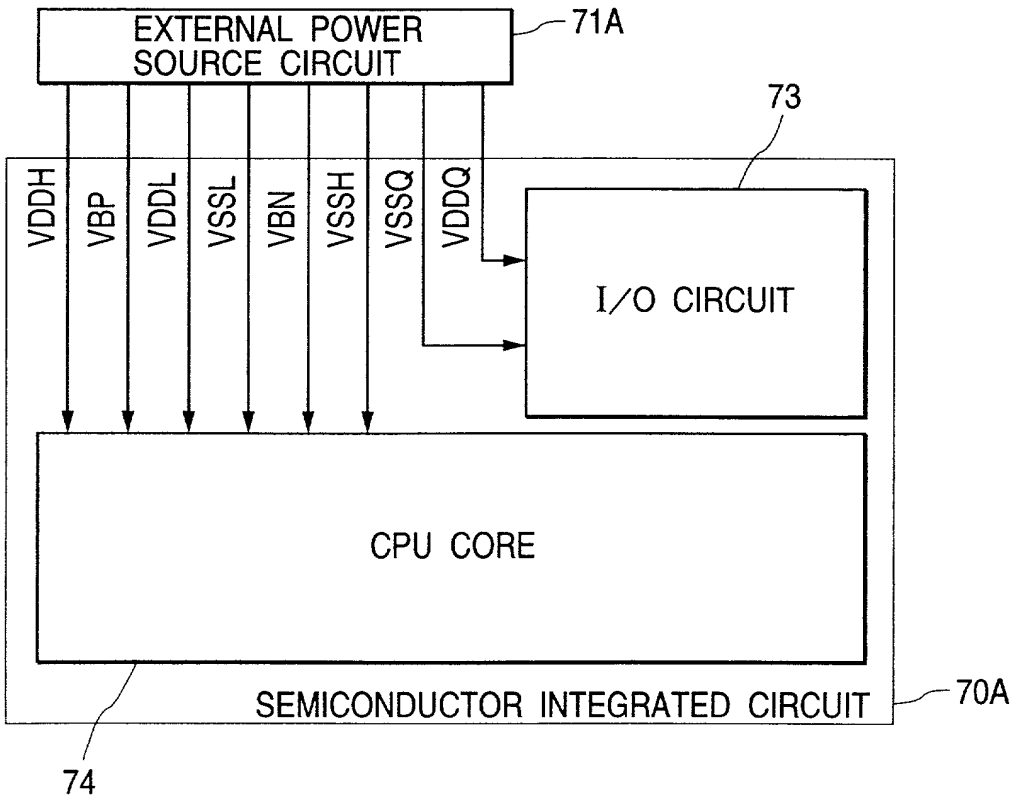

EXTERNAL POWER SOURCE CIRCUIT
71A
73
VDDH
VBP
VDDL
VSSL
VBN
VSSH
VSSQ
VDDQ
I/O CIRCUIT
CPU CORE
SEMICONDUCTOR INTEGRATED CIRCUIT
70A
74

FIG. 24

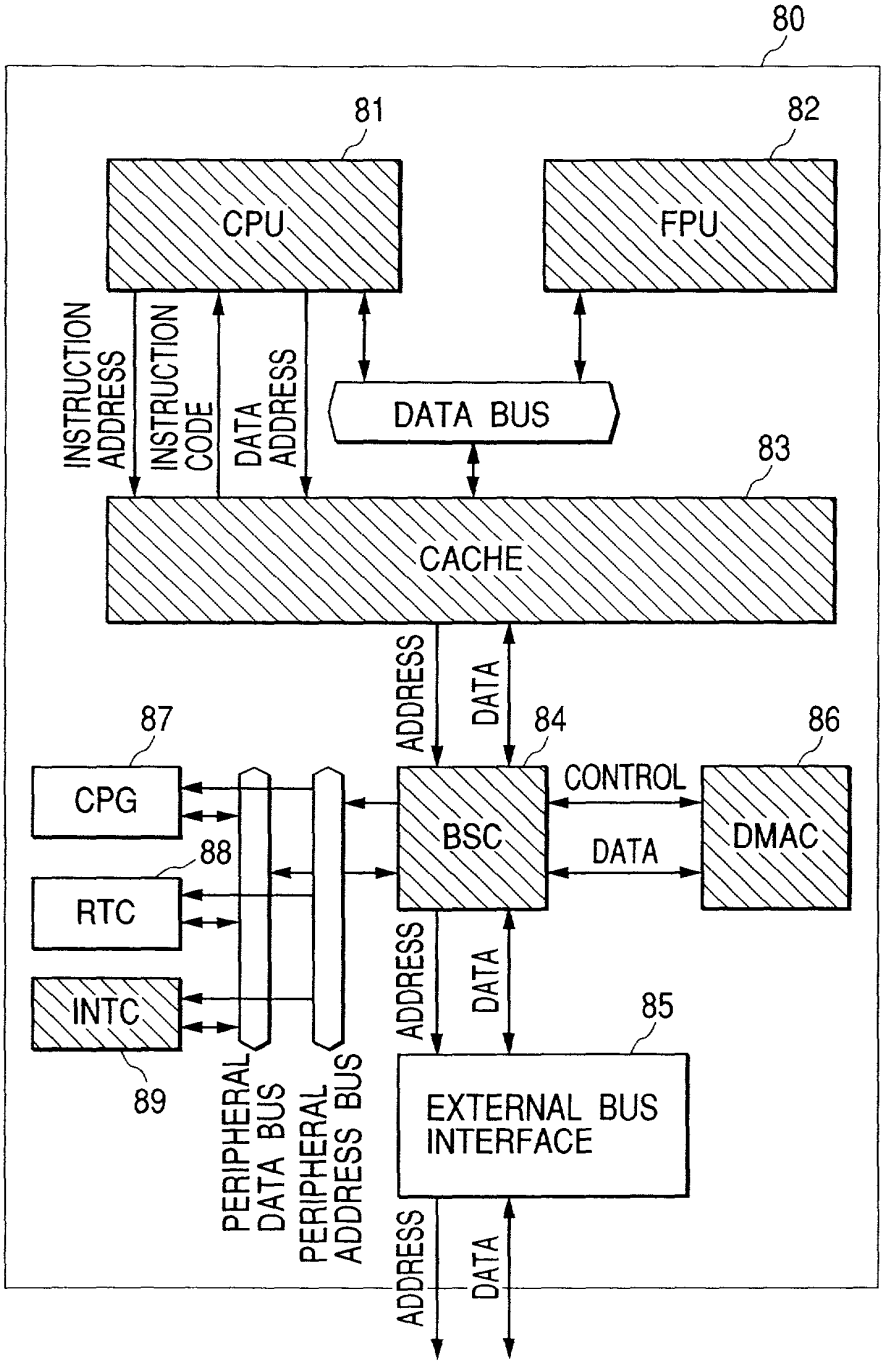

80
81
82
CPU
FPU
INSTRUCTION ADDRESS
INSTRUCTION CODE
DATA ADDRESS
DATA BUS
83
CACHE
ADDRESS
DATA
87
84
86
CPG
CONTROL
BSC
DMAC
DATA
88
RTC
INTC
ADDRESS
DATA
85
89
PERIPHERAL DATA BUS
PERIPHERAL ADDRESS BUS
EXTERNAL BUS INTERFACE
ADDRESS
DATA

FIG. 25

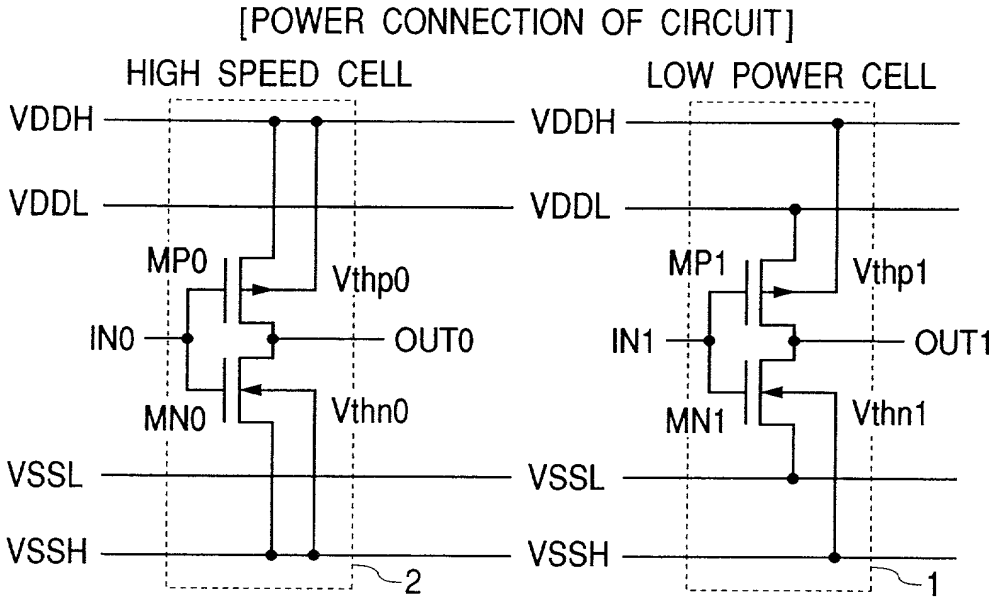

[POWER CONNECTION OF CIRCUIT]
HIGH SPEED CELL
LOW POWER CELL
VDDH
VDDL
MP0
Vthp0
IN0
OUT0
MN0
Vthn0
VSSL
VSSH
2
VDDH
VDDL
MP1
Vthp1
IN1
OUT1
MN1
Vthn1
VSSL
VSSH
1

FIG. 26

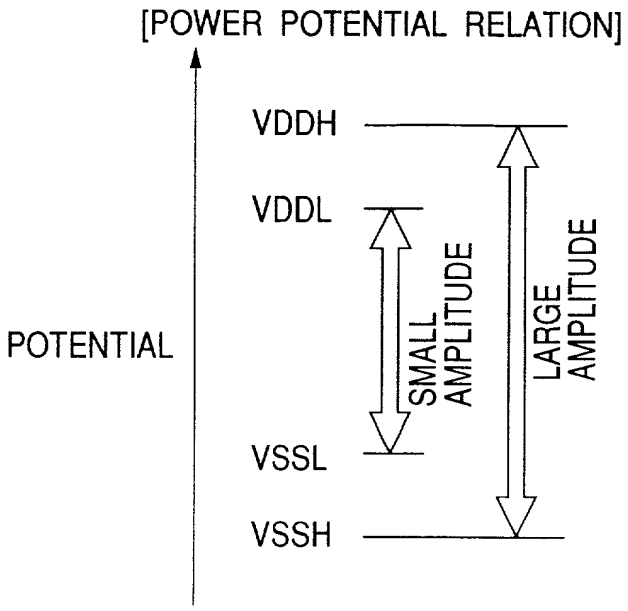

[POWER POTENTIAL RELATION]
POTENTIAL
VDDH
VDDL
VSSL
VSSH
SMALL AMPLITUDE
LARGE AMPLITUDE

FIG. 27

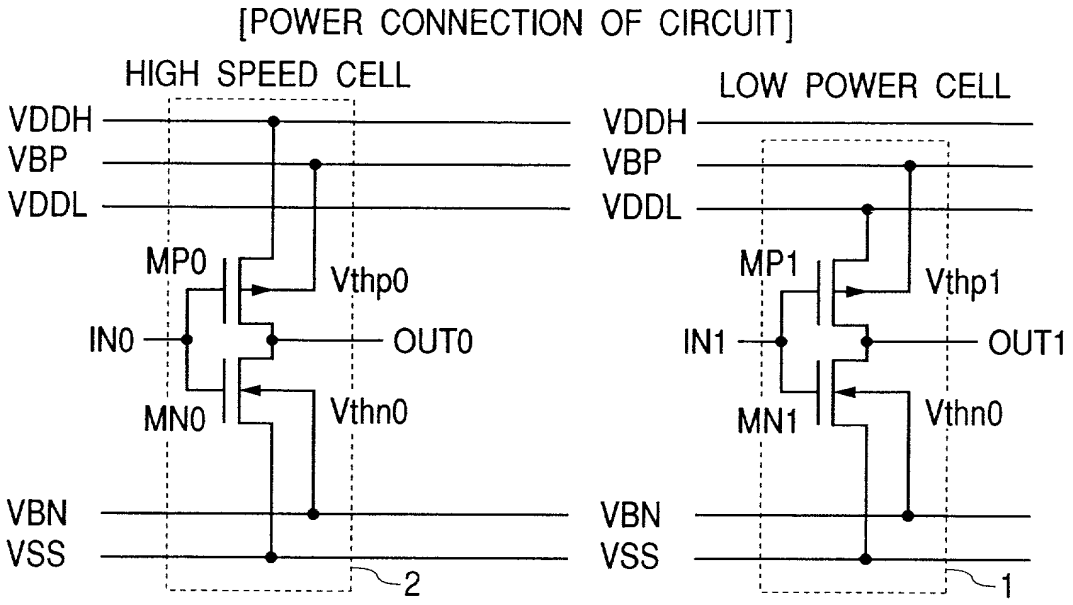

[POWER CONNECTION OF CIRCUIT]
HIGH SPEED CELL
LOW POWER CELL
VDDH
VBP
VDDL
MP0
Vthp0
IN0
OUT0
MN0
Vthn0
VBN
VSS
2
MP1
Vthp1
IN1
OUT1
MN1
Vthn0
1

FIG. 28

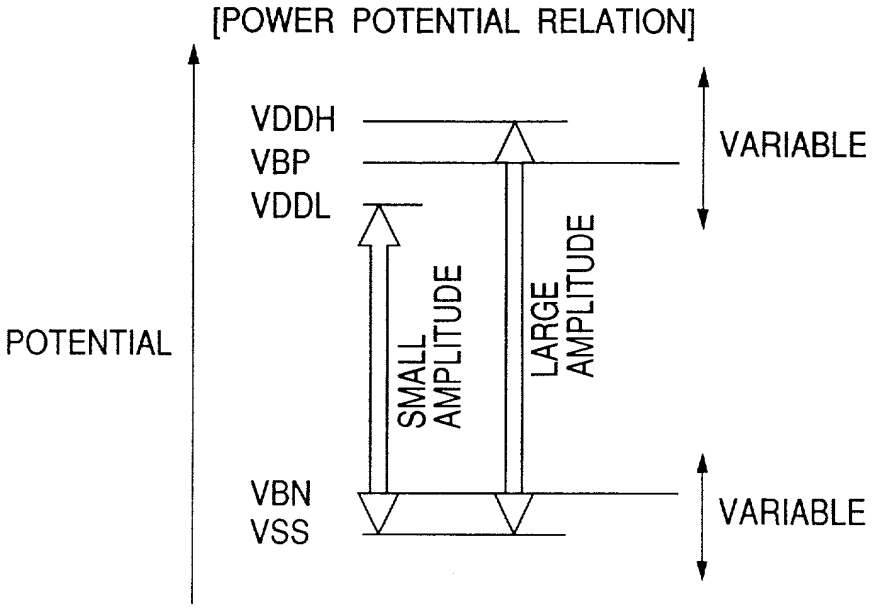

[POWER POTENTIAL RELATION]
POTENTIAL
VDDH
VBP
VDDL
VBN
VSS
VARIABLE
SMALL AMPLITUDE
LARGE AMPLITUDE
VARIABLE

FIG. 29

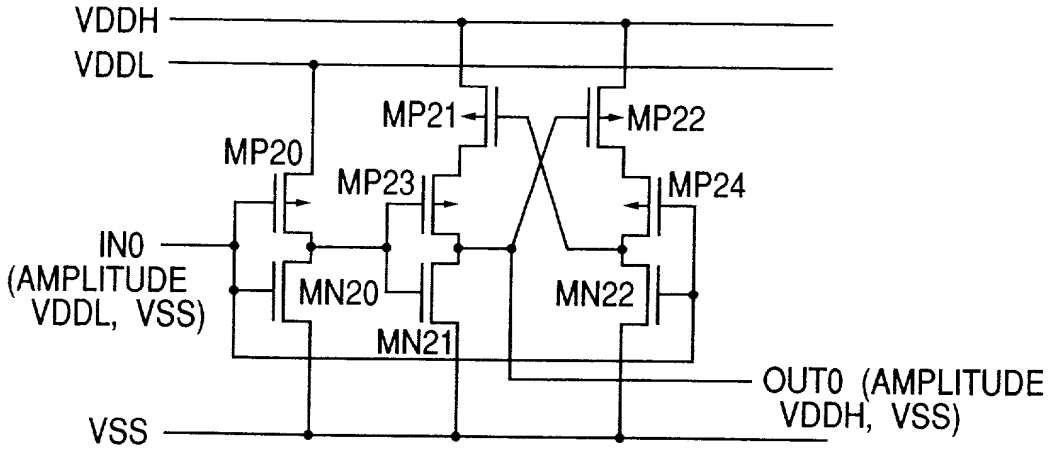
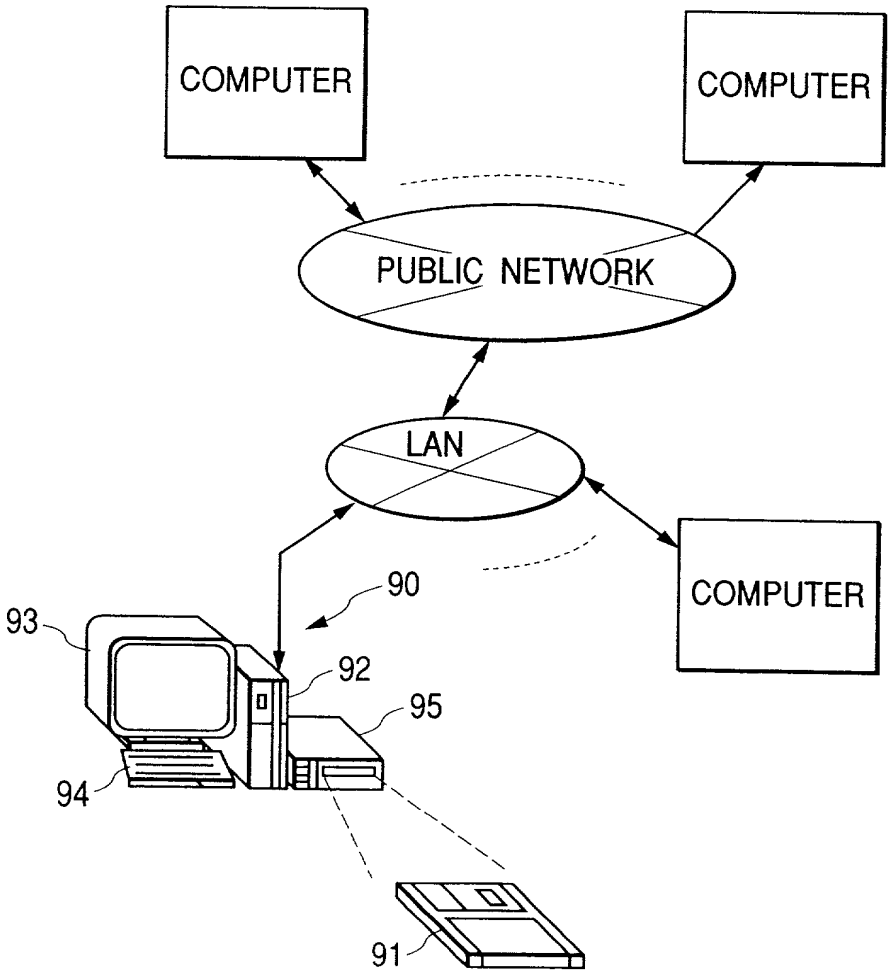

VDDH
VDDL
MP21
MP22
MP20
MP23
MP24
IN0
(AMPLITUDE
VDDL, VSS)
MN20
MN22
MN21
OUT0 (AMPLITUDE
VDDH, VSS)
VSS

FIG. 30


COMPUTER
COMPUTER
PUBLIC NETWORK
LAN
COMPUTER
90
93
92
95
94
91